IN THE CLAIMS

Please amend the claims as noted in the following claim listing:

1. (Currently Amended) A method for determining a bit error rate, comprising the steps of:

acquiring a data signal by an acquisition unit of a test instrument for a predetermined period of time;

storing said data signal in a memory of said test instrument;

recovering a clock signal from said stored data signal by establishing a threshold and determining pairs of adjacent samples of said stored data signal that straddle said threshold, taking into account a hysteresis requirement to confirm that a determined pair of adjacent samples that straddle said threshold represent a threshold crossing point;

slicing said stored data signal into a plurality of data segments of a predetermined length in accordance with said recovered clock signal;

synchronizing each of said data segments to align them to a frame or predetermined pattern to determine a bit error rate thereof; and

comparing each of said data segments to said predetermined pattern on a bit by bit basis.

2. (Currently Amended) The method of processing a data signal of claim 1, wherein said clock recovery step further comprises the steps of:

~~defining a threshold level relative to said stored data signal;~~

comparing each portion of the stored data signal to said threshold level;

~~determining pairs of adjacent samples that straddle said threshold;~~ and

estimating a time of crossing said threshold between said adjacent samples to obtain a series of observed times of threshold crossing.

3. (Original) The method of claim 2, said clock recovery step further comprising the steps of:

comparing said series of observed times of threshold crossing to an ideal perfectly periodic sequence of expected times of threshold crossing comprising said recovered virtual periodic clock;

determining an error between said observed times of threshold crossing and of said series of expected times of threshold crossing comprising said recovered virtual clock based upon said comparison; and

adjusting the phase of said recovered virtual periodic clock in accordance with said determined error.

4. (Original) The method of claim 1, further comprising the steps of:

determining a position of each bit error in a frame; and

displaying said position of each determined bit error in an x/y display of said frame.

5. (Original) The method of claim 1, wherein said predetermined pattern is compared to each of said data segments to determine bit errors therein.

6. (Original) The method of claim 5, wherein if said determined bit rate is extremely high above a predetermined threshold, said alignment between the pattern and the data segments is adjusted.

7. (Original) The method of claim 1, wherein said predetermined pattern is a pseudo-randomly generated bit sequence.

8. (Original) The method of claim 1, wherein said predetermined pattern is a known standard test pattern.

9. (Original) The method of claim 1, wherein said predetermined pattern is a custom test pattern stored in a data file.

10. (Currently Amended) An apparatus for determining a bit error rate, comprising:

an acquisition unit of a test instrument for acquiring a data signal for a predetermined period of time;

a memory of said test instrument for storing said data signal;

a clock recovery unit for recovering a clock signal from said stored data signal by establishing a threshold and determining pairs of adjacent samples of said stored data signal that straddle said threshold, taking into account a hysteresis requirement to confirm that a determined pair of adjacent samples that straddle said threshold represent a threshold crossing point;

a processor for slicing said stored data signal into a plurality of data segments of a predetermined length in accordance with said recovered clock signal;

a synchronizer for synchronizing each of said data segments to align them to a predetermined pattern; and

a bit error tester for comparing each of said data segments to said predetermined pattern on a bit by bit basis to determine a bit error rate thereof.

11. (Currently Amended) The apparatus of claim 10, wherein said clock recovery unit ~~defines a threshold level relative to said stored data signal,~~ compares each portion of the stored data signal to said threshold level, ~~determines pairs of adjacent samples that straddle said threshold,~~ and estimates a time of crossing said threshold between said adjacent samples to obtain a series of observed times of threshold crossing.

12. (Original) The apparatus of claim 11, said clock recovery unit further comparing said series of observed times of threshold crossing to an ideal perfectly periodic sequence of expected times of threshold crossing comprising said recovered virtual periodic clock, determining an error between said observed times of threshold crossing and of said series of expected times of threshold crossing comprising said recovered virtual clock based upon said comparison, and adjusting the phase of said recovered virtual periodic clock in accordance with said determined error.

13. (Original) The apparatus of claim 10, said bit error rate tester determining a position of each bit error in a frame, and displaying said position of each determined bit error in an x/y display of said frame.

14. (Original) The apparatus of claim 10, wherein said predetermined pattern is compared to each of said data segments to determine bit errors therein.

15. (Original) The apparatus of claim 14, wherein if said determined bit rate is extremely high above a predetermined threshold, said alignment between the pattern and the data segments is adjusted.

16. (Original) The apparatus of claim 10, wherein said predetermined pattern is a pseudo-randomly generated bit sequence.

17. (Original) The apparatus of claim 10, wherein said predetermined pattern is a known standard test pattern.

18. (Original) The apparatus of claim 10, wherein said predetermined pattern is a custom test pattern stored in a data file.